

PRIOR ART

FIG. 1

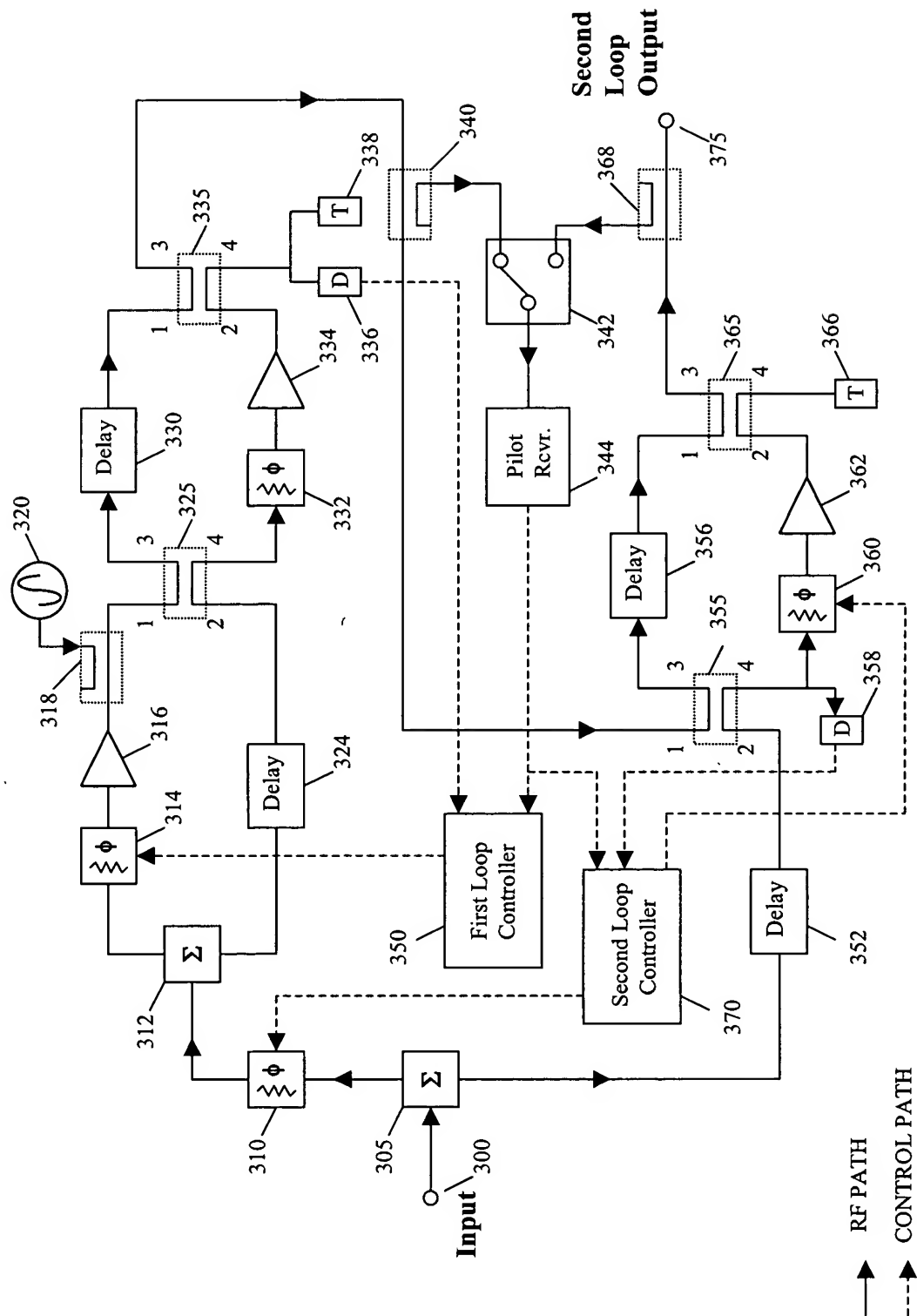
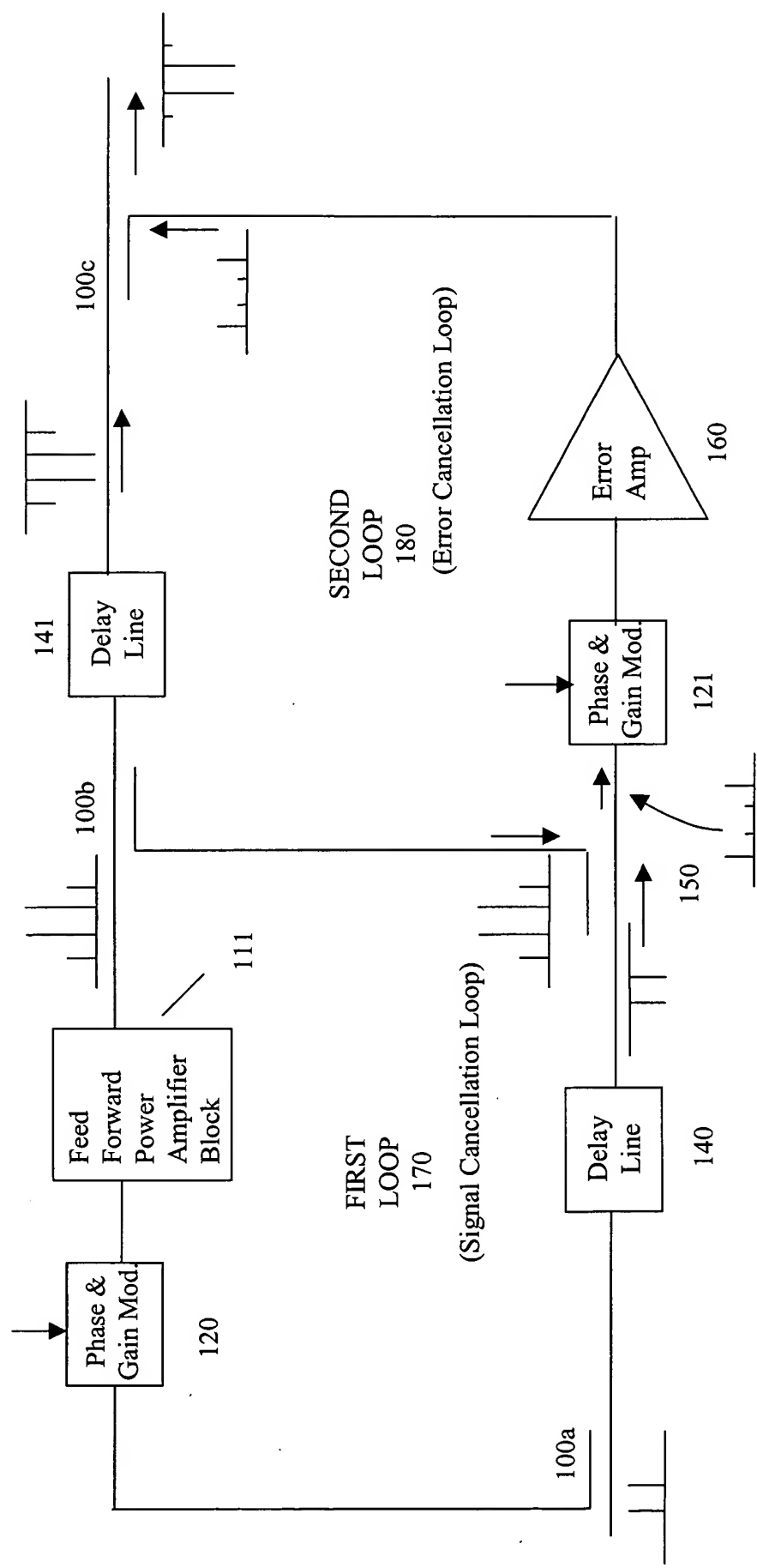


FIG. 2

PRIOR ART



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FIG. 3

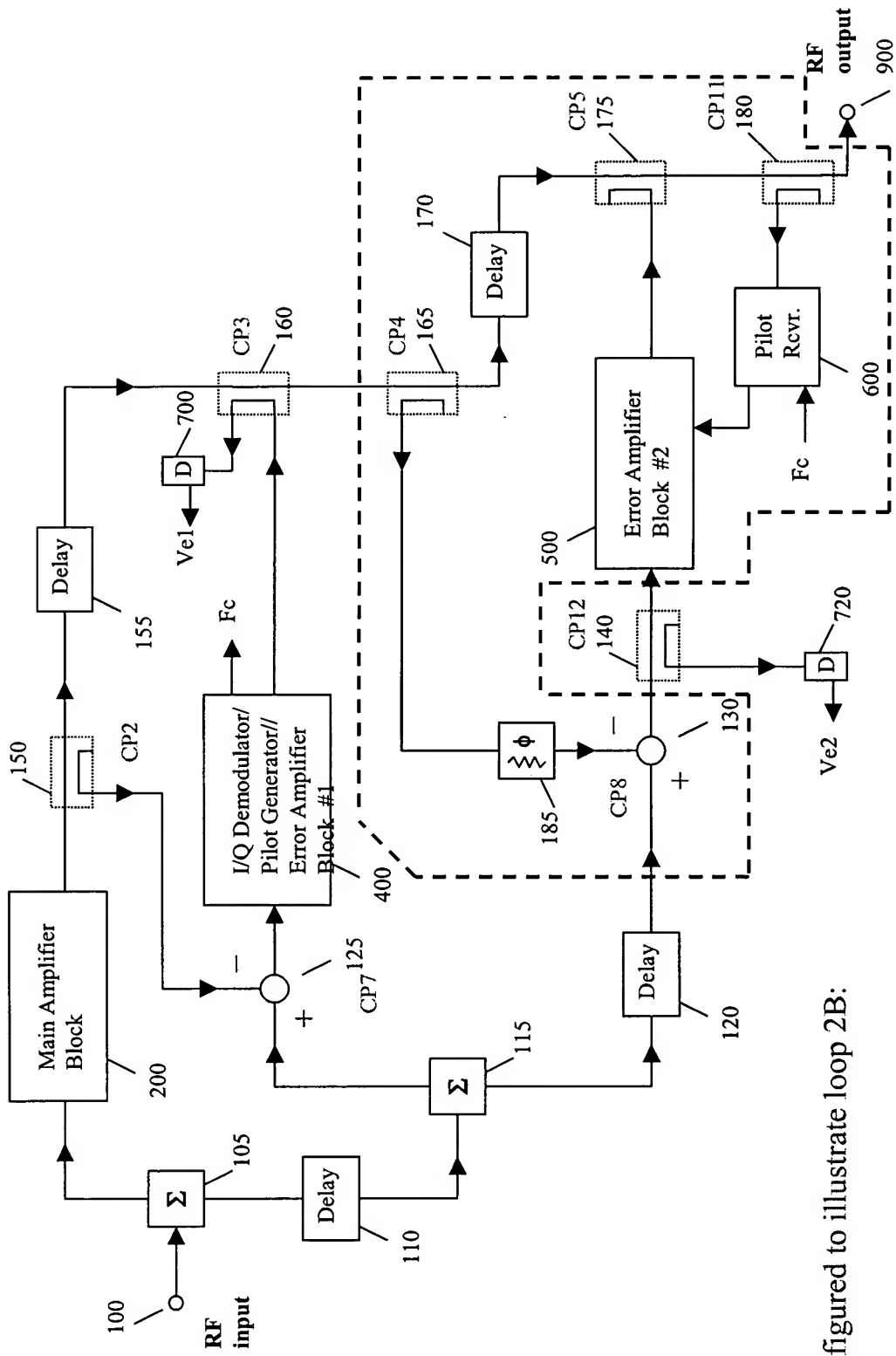


FIG. 4



FIG. 5





configured to illustrate loop 2B:

FIG. 7

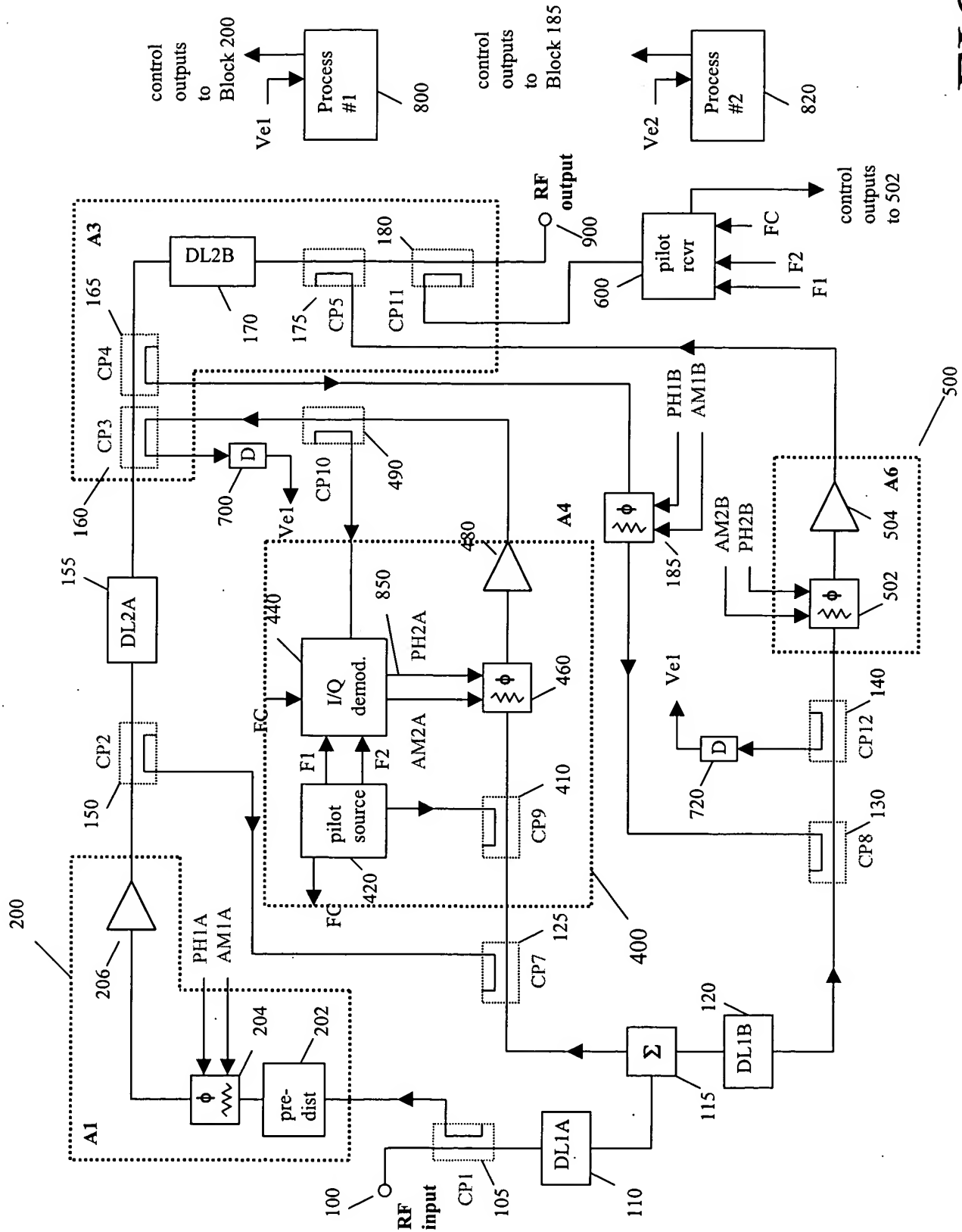


FIG. 8

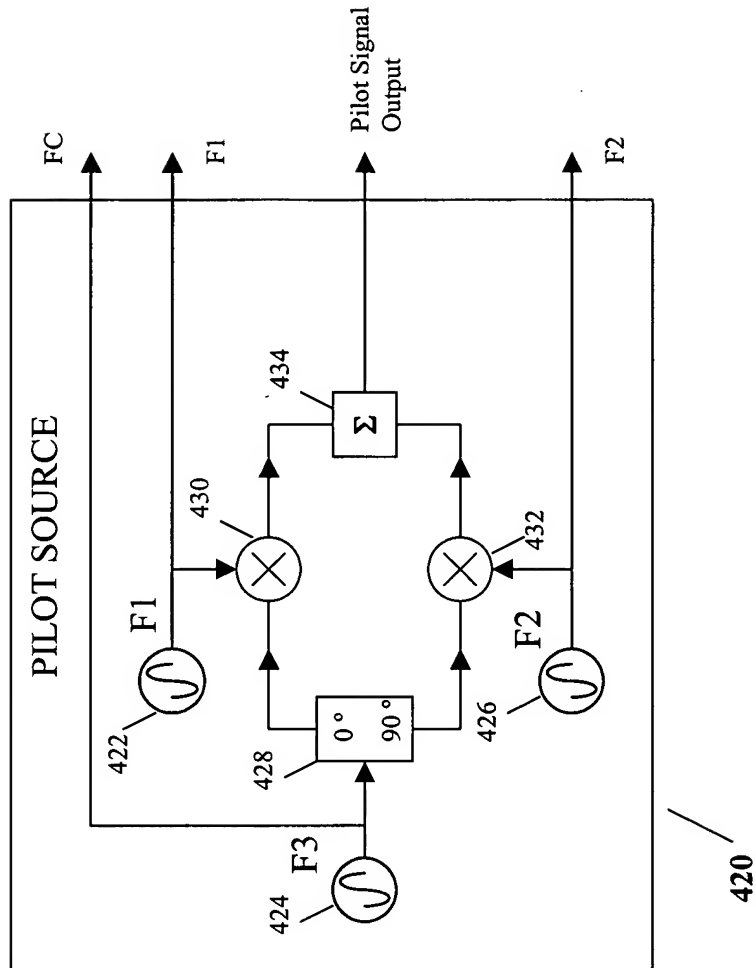


FIG. 9

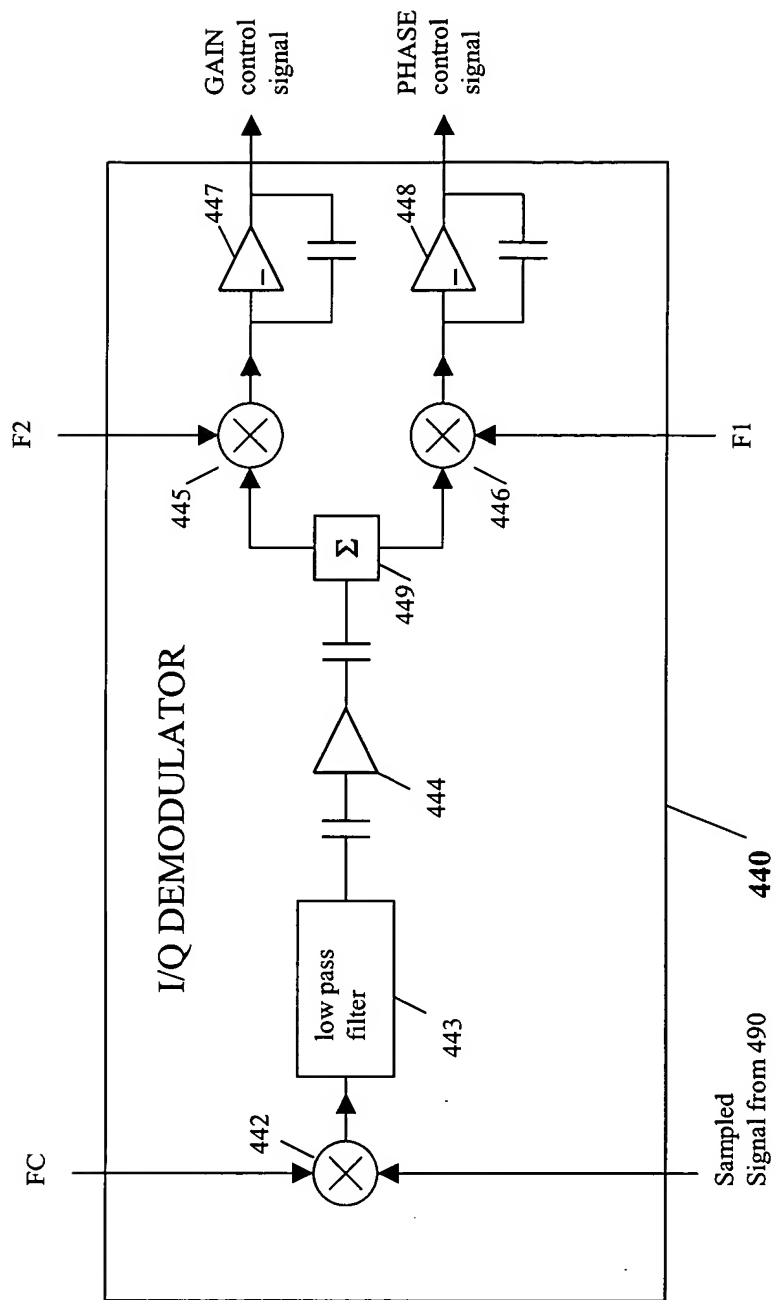


FIG. 10

[illegible]

FIG. 11

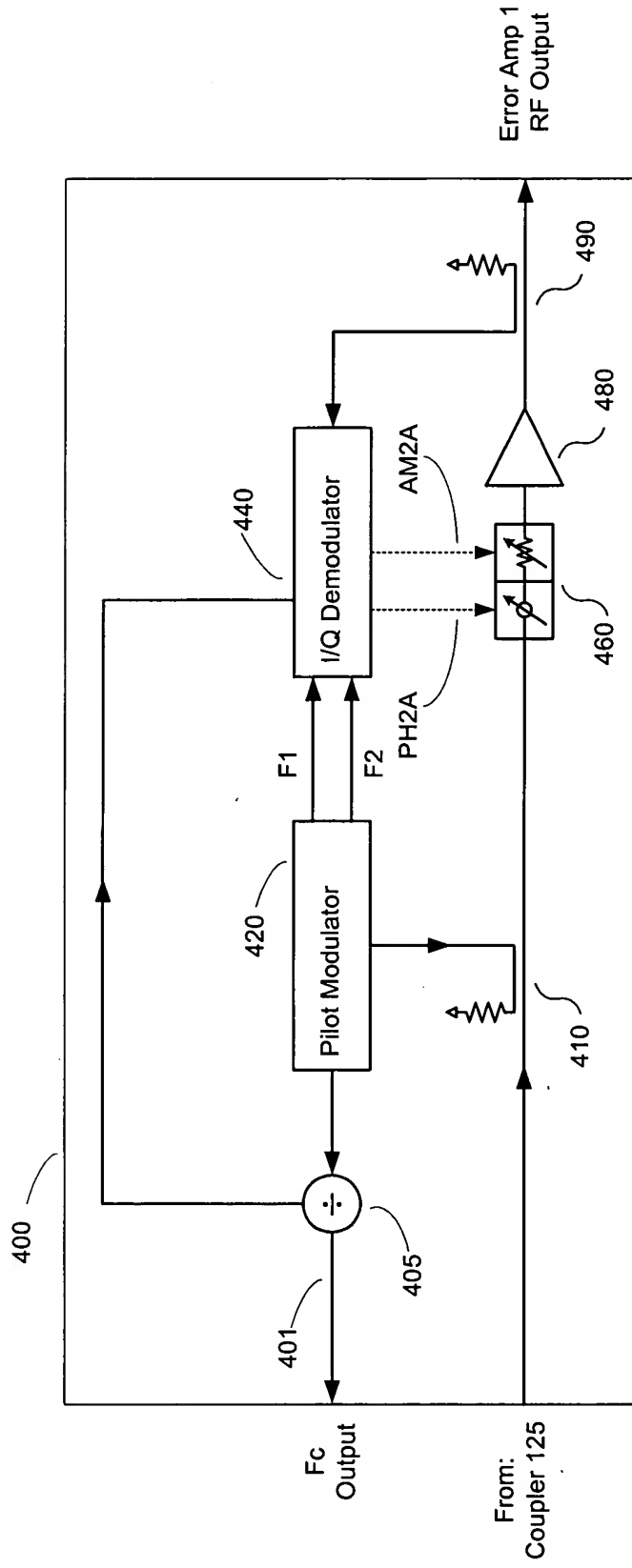
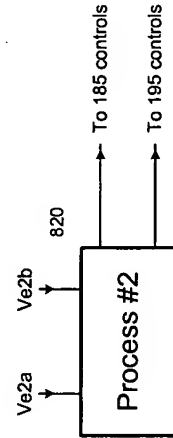


FIG. 12



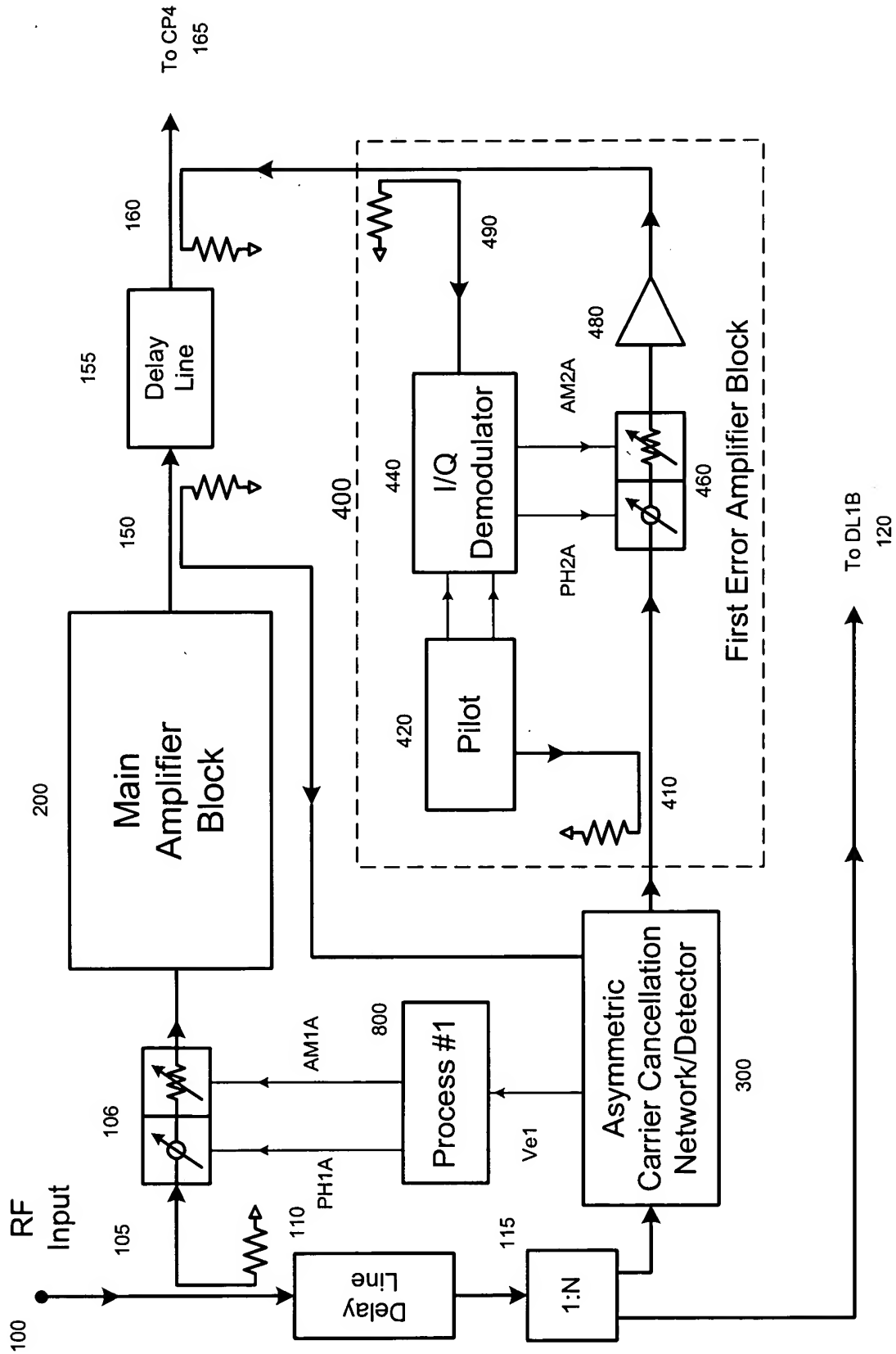


FIG. 13B

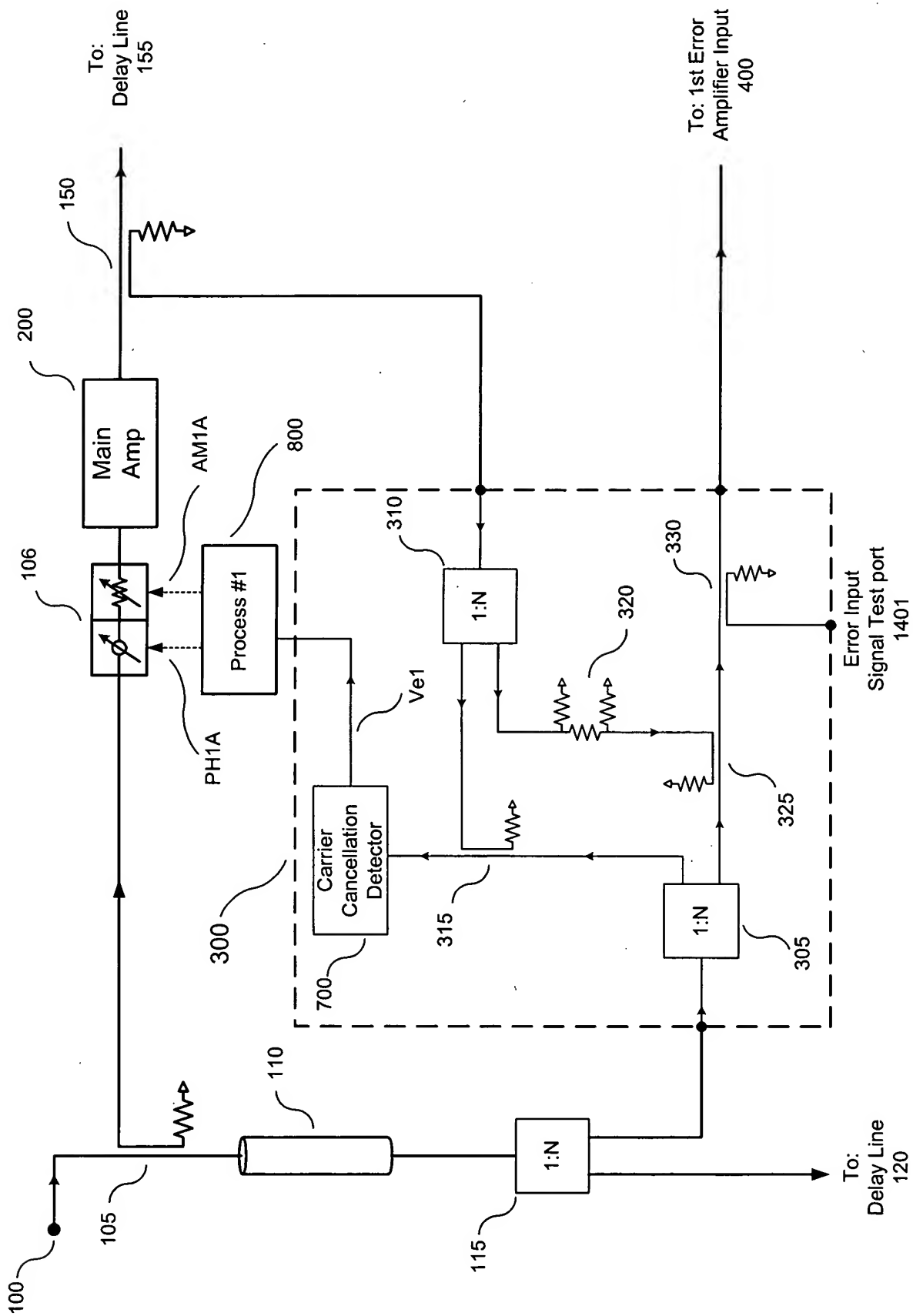


FIG. 14

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Informal Drawings



FIG. 15

Error Amplifier Stabilization

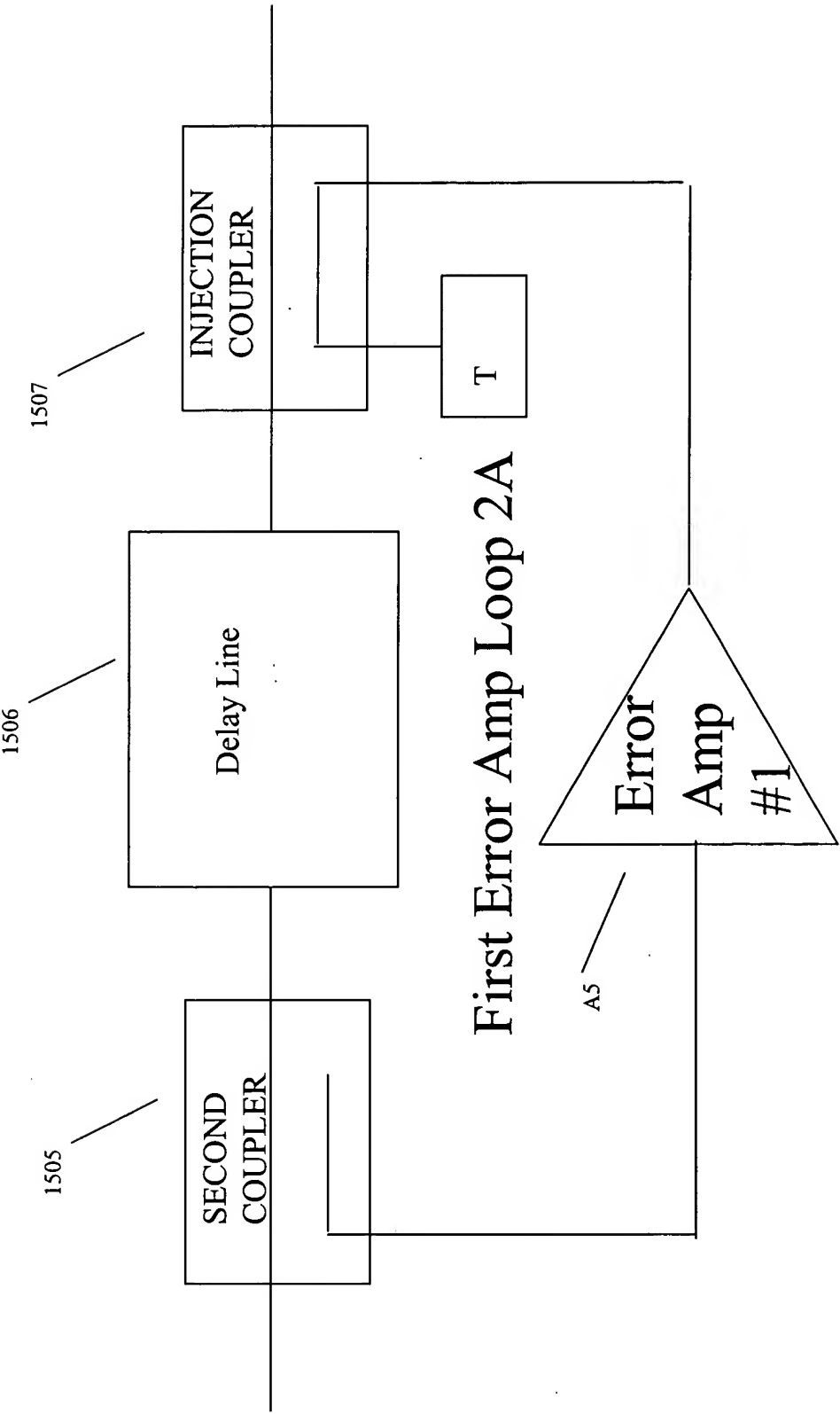


FIG. 16

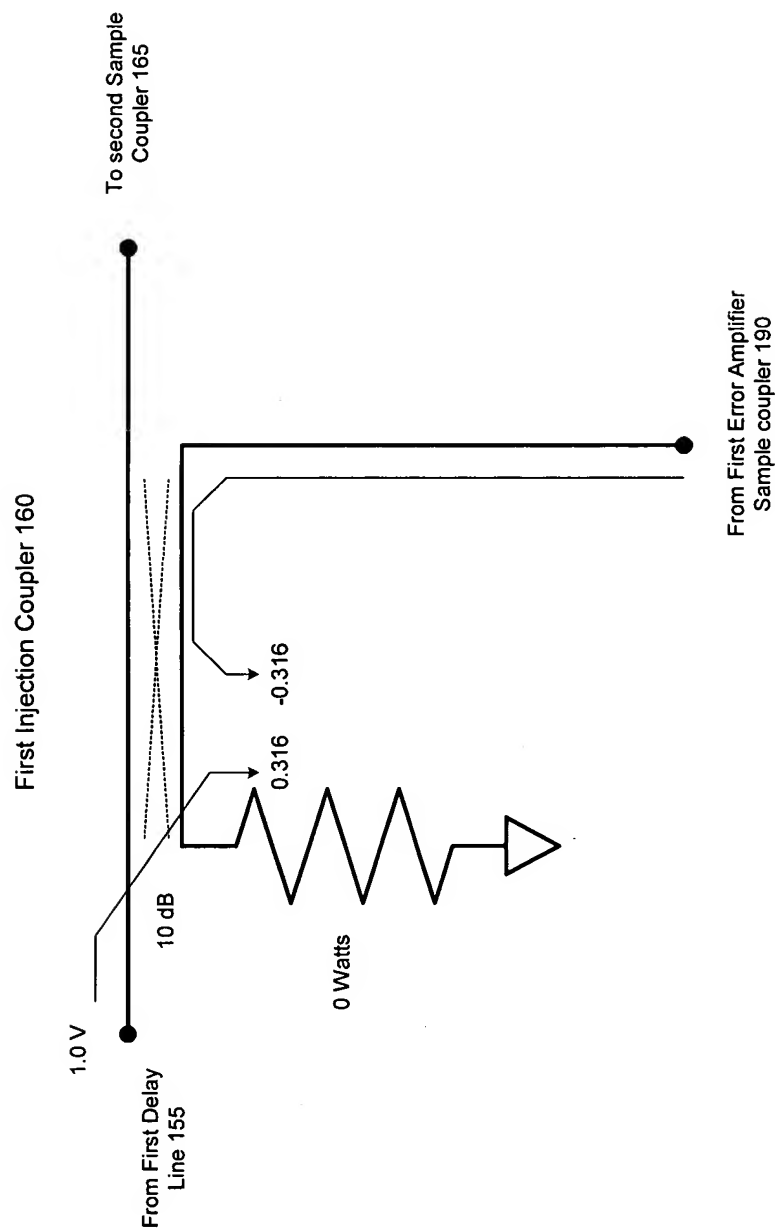


FIG. 17

Carrier Re-Injection

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Informal Drawings

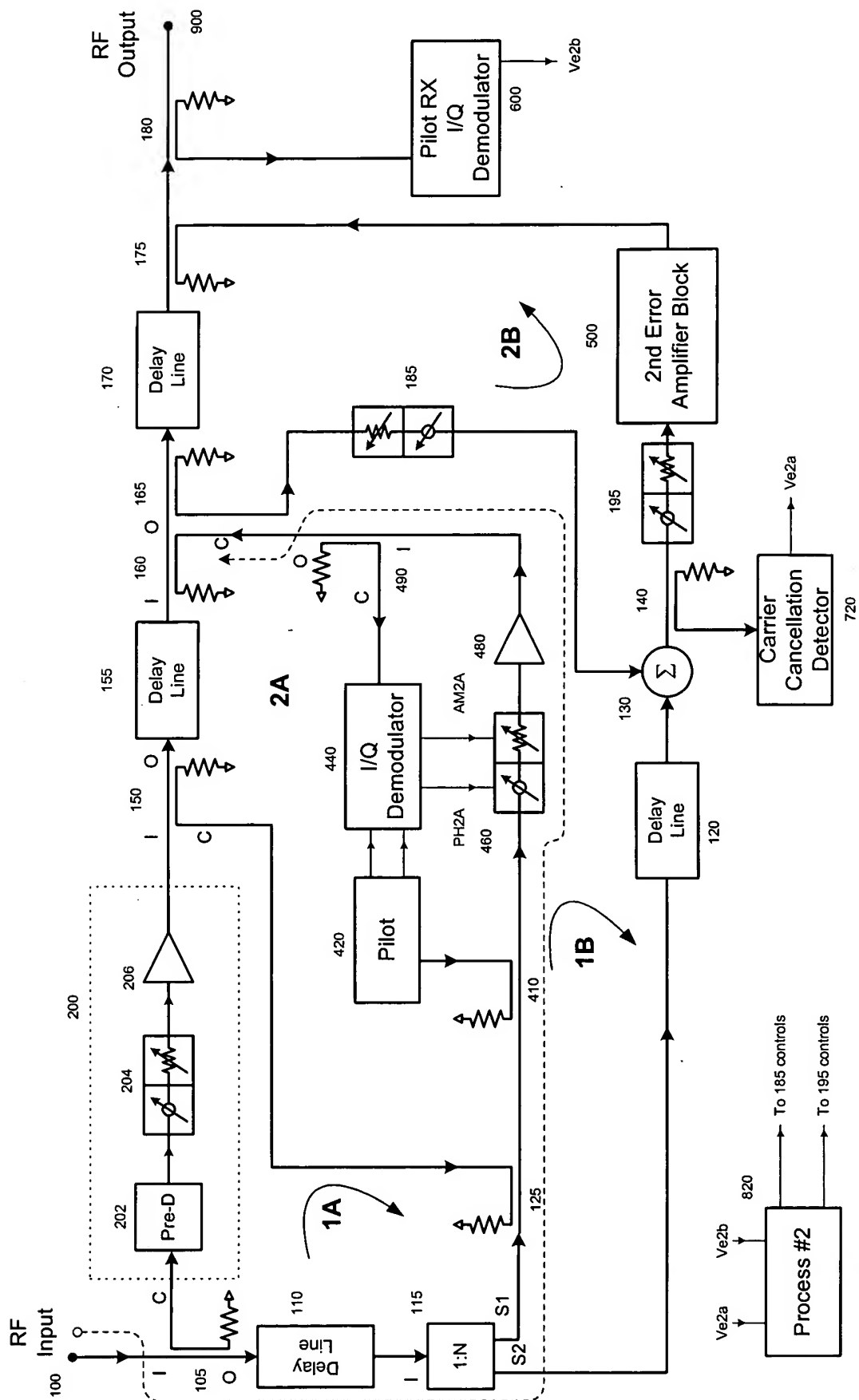


FIG. 18

Originally Submitted
Informal Drawings



FIG. 19